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CLAIMS:

1. A method of forming a trench within a semiconductor substrate, comprising:

providing a semiconductor substrate;

providing a patterned first CVD-deposited masking material layer over said semiconductor substrate, said patterned first masking material layer comprising a first aperture;

depositing a second CVD-deposited masking material layer over said first masking material layer;

etching said second masking material layer until a second aperture is created in said second masking material within said first aperture, said second aperture being narrower than said first aperture; and

etching said semiconductor substrate through said second aperture such that a trench is formed in said semiconductor substrate.

2. The method of claim 1 wherein said patterned first masking material layer is provided over said semiconductor substrate by a method comprising:

providing a first masking material layer over said semiconductor substrate;

applying a patterned photoresist layer over said first masking material layer; and

etching said first masking material layer through an aperture in said patterned photoresist layer such that said first aperture is formed in said first masking material layer.

3. The method of claim 1, wherein said first and second masking material layers are of the same material composition.

4. The method of claim 1, wherein said semiconductor substrate is a silicon substrate.

5. The method of claim 4, wherein said first and second masking material layers are silicon oxide layers.

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6. The method of claim 1, wherein said process of etching said second masking material layer is an anisotropic, dry oxide etching process.

7. The method of claim 1, wherein said process of etching said semiconductor substrate is an anisotropic reactive ion etching process.

8. The method of claim 2, wherein said processes of etching said first and second masking material layers are anisotropic, dry oxide etching processes.

9. The method of claim 2, wherein said photoresist layer is a positive resist layer.

10. The method of claim 1, wherein said first trench mask aperture ranges from 0.4 to 0.8 microns across in smallest dimension and said second trench mask aperture ranges from 0.2 to 0.6 microns across in smallest dimension.

11. A method of forming a trench MOSFET comprising the method of claim 1.

12. A method of forming a trench MOSFET comprising:

providing a semiconductor wafer of a first conductivity type;

depositing an epitaxial layer of said first conductivity type over said wafer, said epitaxial layer having a lower majority carrier concentration than said wafer;

forming a body region of a second conductivity type within an upper portion of said epitaxial layer;

providing a patterned first masking material layer over said epitaxial layer, said patterned first masking material layer comprising a first aperture;

depositing a second masking material layer over said first masking material layer;

etching said second masking material layer until a second aperture is created in said second masking material layer within said first aperture, said second aperture being narrower than said first aperture;

forming a trench in said epitaxial layer by etching said semiconductor wafer through said second aperture;

forming an insulating layer lining at least a portion of said trench;

forming a conductive region within said trench adjacent said insulating layer; and

forming a source region of said first conductivity type within an upper portion of said body region and adjacent said trench.

13. The method of claim 12 wherein said patterned first masking material layer is provided over said semiconductor wafer by a method comprising:

providing a first masking material layer over said epitaxial layer;

applying a patterned photoresist layer over said first masking material layer; and

etching said first masking material layer through an aperture in said patterned photoresist layer such that said first aperture is formed in said first masking material layer.

14. The method of claim 12, wherein said semiconductor wafer is a silicon wafer and said epitaxial layer is a silicon epitaxial layer.

15. The method of claim 12, wherein said first and second masking material layers are of the same material composition.

16. The method of claim 14, wherein said first and second masking material layers are silicon dioxide layers.

17. The method of claim 12, wherein said process of etching said second masking material is an anisotropic, dry oxide etching process.

18. The method of claim 12, wherein said process of etching said semiconductor is an anisotropic, reactive ion etching process.

19. The method of claim 13, wherein said photoresist layer is a positive resist layer.

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20. The method of claim 13, wherein said processes of etching said first and second masking material layers are anisotropic, dry oxide etching processes.

21. The method of claim 12, wherein said first trench mask aperture ranges from 0.4 to 0.8 microns in smallest dimension and said second trench mask aperture ranges from 0.2 to 0.6 microns in smallest dimension.